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EXAMINER J. VOCKRODT – GROUP ART UNIT 2822
DRAFT FOR EXAMINER DISCUSSION PURPOSES

RE: 09/160,657 - INTERVIEW

I am forwarding a draft response for your review in preparation for the interview scheduled fro 10:00am on April 10, 2003 at which I shall be joined by one of the inventors, Dr. Joseph Lyding.

If you have any questions in the meantime, please feel free to telephone me. I shall be leaving Dallas the morning of April 9.

Regards,

N. Rhys Merrett
Tel: 972-862-7428

DRAFTONLY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application: No. 09/160,657 Docket: UIL-10013C

Filed: September 25, 1998 Group Art Unit 2822

Inventor(s):. Joseph W. Lyding et al Examiner: VOCKRODT, Jeff B.

For: SEMICONDUCTIVE DEVICES AND METHODS FOR SAME

Assistant Commissioner of Patents
Washington, D.C. 20231

BOX RCE

CERTIFICATE UNDER RULE 37 CFR 1.8
I hereby certify that the below correspondence is being facsimile transmitted to the United States Patent Office on

Date N. Rhys Merrett

*****DRAFT – FOR DISCUSSION ONLY*****
AMENDMENT UNDER 37 CFR 1.116

This amendment follows the Request for Continued Examination of the application facsimile transmitted on February 10, 2003 and responds to the Final Office Action mailed October 9, 2002. Please enter the following amendments and responsive comments.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Application No. 09/160,157

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 42-46, 48, and 75 (cancelled)

Claim 40. (currently amended) A semiconductor device comprising an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, ~~having~~ an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer, said field effect transistor structurally characterized by the ~~presence~~ retention of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects during operation~~, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress~~.

Claim 41. (previously amended) The semiconductor device of claim 40 wherein said gate insulating layer comprises silicon dioxide.

Claims 42-46 (cancelled)

Claim 47. (previously added) The semiconductor device of claim 40, which is encapsulated.

Claim 48 (cancelled)

Claim 60. (previously amended) The semiconductor device of claim 40, wherein said gate insulating layer comprises an oxide of silicon.

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Claim 61. (previously amended) The semiconductor device of claim 40, wherein said gate insulating layer comprises silicon dioxide or silicon oxy nitride.

Claim 62. (currently amended) A semiconductor device comprising an n-channel field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer having a thickness not exceeding about 55 Angstroms, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by post-fabrication heating of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

Claim 63. (currently amended) The semiconductor device of claim 62 wherein said gate insulating layer comprises silicon ~~dioxide~~oxide.

Claim 64. (currently amended) The semiconductor device of claim 62, wherein said ~~semiconductive silicon layer is a crystalline silicon~~gate insulating ~~layer~~comprises silicon oxynitride.

Claim 65. (previously added) The semiconductor device of claim 62, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.

Claim 66. (previously added) An improved semiconductor transistor device having a transistor gate and a film located adjacent said transistor gate and having a concentration of deuterium within said film, wherein the improvement comprises:

a concentration of at least about 10^{16} cm^{-3} of said deuterium being present in said film, said transistor device susceptible to degradation associated with hot carrier stress, said

concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.

Claim 67 (previously amended) The device as recited in claim 66 wherein said film is a dielectric film, and said transistor gate comprises polysilicon .

Claim 68. (previously added) The device as recited in claim 67 wherein said dielectric film is comprised of a material selected from the group consisting of silicon dioxide, silicon nitride, or silicon oxynitride, each of which includes a substantial concentration of a hydrogen isotope.

Claim 69 (previously amended) The device as recited in claim 68 wherein said transistor gate is comprised of polycrystalline silicon.

Claim 70. (previously added) The device as recited in claim 66 wherein said film is a field oxide, a gate oxide or a dielectric.

Claim 71. (previously added) The device as recited in claim 70 wherein said transistor is a complementary metal oxide semiconductor.

Claim 72. (previously amended) The device as recited in claim 66 wherein said substrate is comprised of a material selected from the group consisting of:
a Group IV element and gallium arsenide.

Claim 73. (previously added) The device as recited in claim 66 wherein said substrate contains at least one doped region.

Claim 74. (previously added) The device as recited in claim 66 further comprising a gate oxide, a field oxide or a spacer, each of which contains a substantial concentration of deuterium.

Claim 75 (cancelled)

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Claim 76. (previously amended) A semiconductor device comprising a field effect transistor having a gate dielectric film having a thickness not exceeding about 55 Angstroms disposed between a transistor gate contact and a semiconductive layer that includes doped source and drain regions and contacts to said doped source and drain regions, said semiconductor device structurally characterized by a concentration of deuterium in said gate dielectric film at an interface with said semiconductive layer provided by heating the device, after formation of said source, drain and gate contacts, at a temperature of about 400°C for about one hour in an atmosphere comprising about 10% deuterium and about 90% nitrogen, said transistor device susceptible to degradation associated with hot carrier stress, and said concentration of deuterium increasing the resilience of the field effect transistor to channel hot carrier stress.

Claim 77. (previously added) A semiconductor device according to claim 76 wherein the semiconductive layer comprises silicon, and the gate dielectric film includes a silicon compound.

Claim 78. (previously amended) A semiconductor device according to claim 77 wherein said silicon compound comprises ~~a~~ an oxygen or a nitrogen containing silicon compound.

Claim 79. (previously added) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, structurally characterized by the gate insulating layer having a thickness not exceeding about 55 Angstroms and by the presence of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature of about 200°C to about 1000°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

Claim 80. (previously amended) A semiconductor device comprising an NMOS field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by said gate insulating layer having a thickness not exceeding about 55 Angstroms and by annealing of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200°C to provide deuterium at said interface between said gate insulating layer and said channel to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

Claim 81. (previously added) An improved semiconductor device including an insulated gate field effect transistor device having a transistor gate and a gate insulator film not exceeding about 55 Angstroms thickness interposed between said transistor and a channel of said transistor device and a concentration of deuterium introduced into and remaining within said film, said transistor device susceptible to degradation associated with hot carrier stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.

Claim 82. (New) An improved semiconductor device according to claim 81, wherein said gate insulator comprises an oxide of silicon.

Claim 83. (New) An improved semiconductor device according to claim 81, wherein said gate insulator comprises silicon oxynitride.

Claim 84. (New) An improved semiconductor device according to claim 81, wherein the field effect transistor comprises an n-channel device subject in operation to hot electron stress.

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REMARKS:

Claims 40, 41, 47, 60, 61, 63-74, 76-79 and 81-84 are now pending in the application for consideration. Claims 42-46, 48, and 75 have been cancelled; claims 40, 62-64 and 80 have been amended and new claims 82-84 have been added.

Claim Rejections – 35 US 112

The Examiner has maintained the rejection of claims 66-74 under 35 US 112, first paragraph, asserting "Applicants must show that the claimed concentration necessarily results from what is described in application S/N 08/586,411 ..." (emphasis in the original). It is believed this condition has been fulfilled. At page 4 lines 17-19 of the Office Action, it is stated "The examiner finds that the example set forth therein [pages 14-18 of the '411 application] only establishes a deuterium anneal that occurs at some point after the gate electrodes of the NMOS transistors are formed – not post-metallization or after the metal contacts are formed." (Emphasis in the original.) With respect, it is maintained that the Examiner's conclusion is incorrect. The annealing of transistor structures under process parameters described at pages 14-18 of the '411 application is identical to those described in *Applied Physics Letters,* 68 (18), pp. 2526-2528, 29 April 1996 (Exhibit A to the affidavit of Dr. Joseph Lyding dated February 6, 2001, and in both cases the transistor structures are identical *Applied Physics Letters* page 2526, paragraph bridging the left and right columns, and Reference No. 6 to that publication, and the '411 application at page 14, lines 15-19, and the post-anneal tests and the test results are identically the same – see '411 application page 17, line 1 to page 18, line 10 and *Applied Physics Letters,* page 2526, right column, first complete paragraph and paragraph bridging pages 2526 and 2527, including the identicality of the gm (transconductance) and threshold voltage (Vth) with time plots shown in Figs. 2 and 3 of the '411 application and Figs. 1 and 2 of *Applied Physics Letters.* Then, in the final paragraph of page 2527 of *Applied Physics Letters* it is stated "*...the replacement of hydrogen with deuterium during the final wafer sintering process results in substantially reduced susceptibility to hot electron degradation effects.*" (Emphasis added). The deuterium annealing process as described in the '411 application at pages 14-18, just as the identical process described in *Applied* Physics, thus occurred after metal contact formation on the transistors, consistent with the disclosure of the Ference article. Consequently, it is believed Applicants have made the requisite showing that the concentration of deuterium in the gate oxide that is described by Ference is an inherent property of

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Applicants' written description and that claims 66-74 are supported by the specification of the '411 application in compliance with 35 US 112. Withdrawal of this ground of rejection of claims 66-74 is believed in order and is respectfully requested, as well as initiation of an interference with U.S. Patent 6,023,093 as previously requested.

Claim Rejections -- 35 US 103

- Claims 40-48, 60-65 and 75-78 have been rejected under 35 US 103 as unpatentable over US Patent 5,514,628 (Enomoto) in view of PCT International Application WO 94/19829 (Lisenker). Claims 42-46, 48, and 75 have been cancelled making the rejection moot in respect of those claims. The rejection is respectfully traversed as to claims 40, 41, 47, 60-65 and 76-78.

The Examiner's rejection is predicated on his opinion that it would have been obvious "to replace the hydrogen of post metallization step in Enomoto, with deuterium as suggested by Lisenker", based on asserted motivation that "comes from Lisenker's teaching that deuterium is superior to hydrogen for increasing device quality and reliability, and that deuterium can be substituted for hydrogen in passivation processes." But this conclusory opinion refutes the Examiner's own concession that Lisenker "does not teach a deuterium annealing step that occurs after electrical contacts have been formed on a semiconductor device." With respect, this is an over expansive interpretation of Lisenker's teaching, unsupported by Lisenker. Lisenker's teaching does not disclose or suggest any beneficial results of deuterium annealing after contact formation, and certainly not "after formation of the circuitry of the integrated circuit" which is an essential feature of Enomoto. The Examiner's position lacks support in Lisenker's disclosure, is not fact based, and is not tenable. The Examiner's proposed combination would be directly contrary to the teaching of Lisenker emphasizing employment of deuterium annealing "in those fabrication steps in which a permanent oxide layer is being formed or treated (Page 8, lines 35-37) and would lack any pertinence to Enomoto. Far from broadly teaching "substituting deuterium as an annealing gas in passivation process", Lisenker teaches only a very narrow and ineffective annealing process limited to fabrication steps prior to contact formation that has no relation to the teaching of Enomoto who mandates hydrogen passivation subsequent to interconnect metallization establishing an integrated circuit. Withdrawal of this ground of rejection is respectfully urged.

- Claims 40-48, 60-65 and 75-81 also have been rejected under 35 US 103 as unpatentable over IEEE Transactions of Electron Devices, Vol 41, No. 12, December 1994, pp 2369-2375 (Okazaki) in view US Patent 5,864,161 (Mitani) and Lisenker. Claims 42-46, 48, and 75 have been cancelled making the rejection moot in respect of those claims. The rejection is respectfully traversed as to claims 40, 41, 47, 60-65 and 76-81.

The limitations of Lisenker's teaching have been discussed above and Lisenker is not seen to have any pertinence to Okazaki's PMOS device. Okazaki teaches improvements in hot carrier reliability by the use of an MBN gate consisting "of a boron-doped and a nitrogen-doped (N-doped) poly-Si double layer" in which "[t]he N-doped Si layer is deposited on the gate oxide by LPCVD." (Page 2369, right column, Section II, first paragraph.) Mitani is seen to add nothing to Okazaki's teaching. Okazaki discloses the use of a forming gas sintering step, widely used during semiconductor device manufacture to improve contact resistivity. This is the same teaching as provided by Mitani; i.e. the passage in Mitani identified by the Examiner discloses annealing, after source/drain electrode patterning, in "a nitrogen atmosphere containing 10% of hydrogen, thereby completing a transistor". Consequently, a person of ordinary skill in the art would have found nothing in Mitani to add to or change Okazaki's teaching. Lisenker's methodology for addressing hot carrier issues is distinct from that taught by Okazaki and Lisenker does not suggest any motivation for dispensing with (nor adding to) Okazaki's own concept of obtaining hot carrier reliability improvement in a PMOS transistor in which hot carrier – hole – degradation problems dominate (see Abstract). In an n-channel device, to which claims 40, 62, 80 and 84 are more particularly directed, hot electron effects dominate. In addition, substitution of Lisenker's teaching for that of Okazaki would have rejected Okazaki's own explicit teaching and would have involved changing the principle of operation of Okazaki which is an impermissible basis for establishing a *prima facie* of obviousness. It is therefore urged that this rejection be withdrawn.

- Claims 40-48, 60-65 and 75-81 also have been rejected under 35 US 103 as unpatentable over IEEE Transactions on Nuclear Science, Vol. 39, No. 6, December 1992, pp. 2220-2229 (Saks) in view of Okazaki. Claims 42-46, 48, and 75 have been

cancelled making the rejection moot in respect of those claims. The rejection is respectfully traversed as to claims 40, 41, 47, 60-65 and 76-81.

Saks teaching is limited to the comparative effects of introducing deuterium and hydrogen into relatively thick MOSFET gate oxides by annealing samples in hydrogen and deuterium, respectively, "after definition of the polysilicon gates and implantation of the N+ source/drains", when the devices were subjected to gamma radiation. Significantly, Saks concludes "There was essentially no effect on the *pre-irradiation* characteristics due to the 900oC D2/H2 annealing, either on the initial Dit value ... or the initial FET threshold voltages." (Page 2221, left column, Section II, second paragraph.) Thus, Saks teaching would have pointed a person of ordinary skill in the art away from the invention claimed in claims 40, 41, 47, 60-65 and 76-81.

Saks concluded that after gamma radiation, "post-irradiation Dit growth rate is clearly retarded in the deuterated oxides compared to the hydrogenated oxides and un-annealed reference oxides." (Page 2227, Section V, first paragraph.) While post deuterium anneal irradiation is a necessary ingredient of Saks' experiment it has no relation to the invention claimed in claims 40, 41, 47, 60-65 and 76-81 of the present application and this disclosure by Saks would not have suggested the claimed invention.

Saks also discusses a deuterium sintering step subsequent to "deposition of the aluminum metalization" and concludes "sintering had no discernable effect on the radiation sensitivity of any of the three oxide types", i.e. un-annealed, hydrogen treated, and deuterium treated. (Page 2222, right column, Section II D., third paragraph. Emphasis added.) Consequently, Saks teaches only that in the context of his experiment no significant changes on radiation sensitivity result and this is not pertinent to the invention claimed in this application. Contrary to the Examiner's assertion, Saks is not seen to disclose any degradation mechanism other than irradiation and his teaching would not have suggested pertinence to MOS device degradation resulting from hot carrier effects, in particular hot electron effects, to the alleviation of which the invention claimed in claims 40, 41, 47, 60-65 and 76-81 of this application is directed, and which are not concerned with radiation sensitivity.

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In summary, Saks suggests that deuterium annealing prior to contact formation is not effective per se, that such annealing followed by deuterium sintering after metallization produces insignificant benefits, and Saks does not teach or suggest effectiveness of deuterium annealing on device degradation due to hot carrier, in particular hot electron, effects.

The Examiner also asserts: "Saks teaches that transistors annealed in deuterium (D2) exhibit 3.2 to 4.5 fold retardation factor relative to transistors annealed in hydrogen (H2) (Saks, Table 1, page 2224)." Saks states that the estimated accuracy of the retardation factors in Table 1 is about +-25% and cautions because of this large experimental uncertainty it is unclear how much of the measured variation is real (Saks, page 2224, right column). This is about the same isotope mass effect as asserted by Lisenker (Lisenker, page 7, line 30 to page 8, line 12). In contrast, the specification of the present application discloses a typical isotope effect of 10 (page 22, line 21 to page 23, line 3) in a MOS device embodying the claimed invention. This enhanced isotope effect results from post gate contact deuterium annealing in combination with a thin gate insulator (not exceeding about 55 Angstroms) and there is no recognition or suggestion in the cited references of the desirability of such a combination of features nor of the problem solved and the benefits of reduced hot carrier (electron) degradation in a device embodying the invention.

Apart from the lack of relevance of Saks as discussed above, Saks does not suggest any motivation for rejecting and dispensing with (nor adding to) Okazaki's own teaching (discussed above in relation to Lisenker) to use an MBN gate consisting "of a boron-doped and a nitrogen-doped (N-doped) poly-Si double layer" in which "[t]he N-doped Si layer is deposited on the gate oxide by LPCVD." (Page 2369, right column, Section II, first paragraph.)

The fact that thin gate insulator devices were, per se, known at the time of the invention is not pertinent to the issue of patentability of claims 62 –65, and 76-81. What is pertinent is that there was no teaching or suggestion in the prior art that disclosed or would have suggested recognition of the desirability of, or the benefits to be obtained by, use of such a thin gate insulating layer in combination post gate contact annealing in deuterium to produce such a profound improvement in device degradation due to hot carrier effects, as evidenced by an isotope effect of 10 exemplified in Applicant's specification. Okazaki proposed a particular gate

insulator structure to address hot hole degradation in a PMOS transistor and neither Lisenker nor Saks provides any motivation for that technique to have been rejected. Uchiyama et al. "High Performance Dual-gate Sub-halfmicron CMOSFETs with 6nm-thick Nitrided SiO2 Films in an N2O Ambient", IEDM Technical Digest, pp. 425-427, 1990 (cited in the accompanying Information Disclosure Statement) discusses 6nm gate oxide thickness CMOSFETs incorporating N2O nitrided gate dielectric films to block boron penetration and to reduce electron traps. Again, neither Lisenker nor Saks provides any motivation for that technique to have been rejected.

Prima facie obviousness

The Examiners' asserted justifications for motivation to combine references in the 35 US 103 rejections appear to be conclusory opinions lacking factual basis in the prior art. As the Examiner is aware, the fact that references could hypothetically be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination. Even the existence of references that taught all individual aspects of a claimed invention is not sufficient to establish a *prima facie* case of obviousness without some objective reason in the prior art to combine the teachings of the references. Each reference must be considered as a whole in the context of its teaching, not on the basis of an arbitrarily selected feature - MPEP 2143.01. With respect, the Examiner has made no such factual showing suggested by the prior art. As demonstrated in the above discussion, not only do the references fail to disclose or suggest desirability for their combination in the manner asserted in the grounds of rejection, they do not, each considered as a whole, disclose, teach or suggest the combination of features set forth in claims 40, 41, 47, 60-65 and 76-81, each considered as a whole. Consequently, the grounds asserted in the Office Action are believed inadequate to sustain rejection of those claims under 35 US 103.

CONCLUSION:

It is believed this amendment and response addresses and overcomes all outstanding grounds of rejection, places all pending claims in condition for allowance, and satisfy the requirements for declaration of an interference with U.S. Patent 6,023,093. Favorable responsive action will be appreciated.

If after consideration, the Examiner believes that any outstanding matters remain, a telephone call to the undersigned attorney at 972-862-7428 will be appreciated.

Respectfully submitted,

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